

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
TI-23686.1

Total Pages in this Submission
32

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

INTEGRATED CIRCUIT HAVING INDEPENDENTLY FORMED ARRAY AND PERIPHERAL ISOLATION DIELECTRICS

and invented by:

CETIN KAYA

jc836 U.S. PTO
09/620649

If a CONTINUATION APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 09/168,047

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

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☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 23 pages and including the following:
 - a. ☒ Descriptive Title of the Invention
 - b. ☐ Cross References to Related Applications (if applicable)
 - c. ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
 - d. ☐ Reference to Microfiche Appendix (if applicable)
 - e. ☒ Background of the Invention
 - f. ☒ Brief Summary of the Invention
 - g. ☒ Brief Description of the Drawings (if drawings filed)
 - h. ☒ Detailed Description
 - i. ☒ Claim(s) as Classified Below
 - j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
- a. ☐ Formal Number of Sheets _____
- b. ☒ Informal Number of Sheets 5
4. ☒ Oath or Declaration
- a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
- b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
- c. ☒ With Power of Attorney ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application,
see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied
under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby
incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy *(identical to computer copy)*
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certificate of Mailing
- ☐ First Class ☐ Express Mail *(Specify Label No.):* _____

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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	9	- 20 =	0	x \$18.00	\$0.00
Indep. Claims	1	- 3 =	0	x \$78.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$690.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$690.00

- ☐ A check in the amount of _____ to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 20-0668 as described below. A duplicate copy of this sheet is enclosed.
- ☒ Charge the amount of \$690.00 as filing fee.
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 - ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
 - ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Jay M. Cantor
Reg. No. 19906
(202) 639-7713

Dated:

cc:

TECHNICAL FIELD OF THE INVENTION

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BACKGROUND OF THE INVENTION

One type of modern nonvolatile memory is the EPROM or EEPROM device that uses floating gate structures. These floating gate memory structures may be integrated into a floating gate array which facilitates interface between the memory cells, control circuitry and high-voltage power sources. The memory cells use channel hot electrons for programming from the drain side and use Fowler-Nordheim tunneling for erasure from the source side. Due to the high voltages frequently used to program and erase the cells, high-voltage peripheral transistors may be implemented to provide an interface between a high-voltage source and the memory cells of the floating gate array. The control logic circuitry of the floating gate array typically functions with a lower operating voltage. Low-voltage peripheral transistors may be implemented to provide the logic circuitry for the array.

It is often desirable to fabricate peripheral transistors and the floating gate memory cells on a common semiconductor substrate. To ensure that each cell operates independently, regions of isolation dielectric may be formed between cells to electrically isolate the gates from one another. Typically, the isolation dielectrics for the memory cells are formed at the same time and are of the same construction as the isolation dielectrics for the periphery^{al} transistors. In addition, to ensure appropriate coupling coefficients, the distal ends of floating gates in the memory cell area are made to overlap the isolation dielectric. The proper voltage applied to the control gate is proportional to the coupling coefficient of the device. Providing overlap of the ends of the floating gates over the isolation dielectric increases the coupling coefficient, allowing for a lower control gate voltage.

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This approach has several disadvantages. One problem with this approach is that it is difficult to instill unique characteristics into the separate isolation dielectrics because they are formed contemporaneously. For example, memory cells frequently use high voltages for programming and erasing data. Periphery transistors interfacing high voltage sources typically implement thicker gate oxides and larger isolation dielectric regions than those typically associated with memory cell gate oxides. Additionally, as memory cell sizes are reduced, their corresponding gate oxides become thinner and isolation dielectric regions become smaller. An approach that contemporaneously forms isolation dielectrics for memory cells and peripheral transistors cannot satisfy these diverging specifications.

Another problem with this approach is that as the memory cells are scaled, they become intolerant to low levels of leakage current. The read current of each memory cell is directly proportional to the area of substrate supporting the floating gate, and inversely proportional to the thickness of the oxide separating the substrate and the floating gate. To facilitate integration with other scaled system elements, the width of the floating gates is frequently decreased. Maintaining a desired overlap of the floating gate over the isolation dielectric, however, requires a corresponding decrease in the substrate area supporting the gate. Decreasing this area width without reducing the gate oxide thickness results in degradation of the cell's read current. To maintain a desired read current, therefore, the thickness of the gate oxide must also decrease. Unfortunately, it is often impractical to decrease the gate oxide thickness because this leads to high levels of stress-induced leakage current. Therefore, it is difficult to scale these devices without either

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SUMMARY OF THE INVENTION

In accordance with the teachings of the present invention, an integrated circuit having independently formed array and peripheral isolation dielectrics is provided that substantially eliminates or reduces the disadvantages associated with the prior techniques and processes.

According to one embodiment of the present invention, a method of forming an integrated circuit comprises forming a first dielectric layer disposed outwardly from a semiconductor substrate and forming a first intermediate structure outwardly from the first dielectric layer. The first intermediate structure comprises a floating gate layer disposed outwardly from the first dielectric layer, a second dielectric layer disposed outwardly from the floating gate layer and a first polysilicon layer disposed outwardly from the second dielectric layer. Next, regions of the first intermediate structure are removed to form at least one gate stack disposed outwardly from the substrate. After the formation of the gate stacks, at least one dielectric isolation region is formed between two gate stacks.

The invention has several important technical advantages. The dielectric isolation regions of the array are formed independently of the peripheral dielectric regions. Peripheral dielectric regions may be formed to a desired thickness for high voltage devices, while array dielectric regions may be scaled to minimize cell size. Additionally, the invention eliminates overlap between the distal ends of the floating gates and the isolation dielectric residing between the gates. The area of substrate supporting each floating gate may be maintained or increased despite the scaling of the floating gate width. A good read current is, therefore, maintained

without creating stress-induced leakage current by thinning the gate oxide layer. Eliminating overlap between the floating gates and the isolation dielectric also facilitates creation of floating gates with little or no topography, making it easier to remove all polysilicon from between the floating gates. Use of relatively flat polysilicon layers solves problems associated with floating gate shorts caused by residual polysilicon residing between the floating gates. Also, because the floating gates do not extend beyond the trench corners, problems associated with oxide thinning such as nonuniformities in data retention and threshold voltages are reduced or eliminated.

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BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the teachings of the present invention may be acquired by referring to the accompanying figures in which like reference numbers indicate like features and wherein;

FIGURE 1 is a cross-sectional view of a portion of one embodiment of an integrated circuit having independently formed array and peripheral isolation dielectric regions according to the teachings of the present invention;

FIGURE 2 is a cross-sectional view of a portion of another embodiment of an integrated circuit having independently formed array and peripheral isolation dielectric regions according to the teachings of the present invention;

FIGURES 3a-3d are a series of cross sectional views showing a portion of a partially completed integrated circuit having independently formed array and peripheral isolation dielectric regions constructed according to the teachings of the present invention; and

FIGURES 4a-4d are a series of cross-sectional views showing a portion of a partially completed integrated circuit having independently formed array and peripheral isolation regions completed according to the teachings of the present invention.

FIGURE 1 is a cross-sectional view of a portion of an integrated circuit 10 having independently formed array and peripheral isolation dielectric regions according to the teachings of the present invention. Integrated circuit 10 comprises a semiconductor substrate 12. A first dielectric layer 20 may be disposed outwardly from an array region 11 of integrated circuit 10. A peripheral dielectric layer 60 may be disposed outwardly from a peripheral region 13 of integrated circuit 10. First dielectric layer 20 and peripheral dielectric layer 60 may comprise, for example, layers of oxide. Other dielectric materials besides oxide may be used to form first and peripheral dielectric layers 20 and 60. First dielectric layer 20 may form a tunnel oxide layer for a floating gate array of memory cells subsequently formed in array region 11. Peripheral dielectric layer 60 may form a gate oxide layer for peripheral transistors subsequently formed in peripheral region 13.

Gate stacks 22 are disposed outwardly from substrate 12 and are separated from substrate 12 by first dielectric layer 20. Each gate stack 22 comprises a floating gate body 24 disposed outwardly from first dielectric layer 20. Each gate stack 22 further comprise a first polysilicon body 26 disposed outwardly from floating gate body 24 and separated from floating gate body 24 by a second dielectric region 28. Second dielectric region 28 may comprise any suitable dielectric material or combination of dielectric materials. Second dielectric region 28 may comprise, for example, oxide, nitride or a heterostructure comprising alternate layers of oxide and nitride. Dielectric isolation regions 30 may reside between gate stacks 22. Each dielectric isolation region may comprise an isolation oxide layer 32 disposed outwardly from the sidewalls of

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FIGURE 2 shows another method of increasing the capacitance between a floating gate 124 and a first polysilicon body 126 of an integrated circuit 100. The capacitance between floating gate body 124 and first polysilicon layer 126 is directly proportional to the surface area of these two bodies. The capacitance between the two gate bodies may, therefore, be increased by increasing the surface area of one or both structures. The effective surface area of floating gate body 124 and first polysilicon body 126 may be increased by forming a hemispherical grain poly layer 110 outwardly from floating gate 124. Hemispherical grain poly layer 110 creates a rough surface outwardly from floating gate 124. Forming second dielectric region 128 outwardly from hemispherical grain poly layer 110 creates a rough surface on second dielectric region 128 during its formation. The rough surface on second dielectric region 128, in turn, creates a rough surface on first polysilicon body 126 when it is formed. The rough surface of first silicon body 126 creates additional effective surface area between floating gate body 124 and first polysilicon body 126, which increases the capacitance between these bodies, resulting in a higher coupling coefficient.

In another embodiment (not explicitly shown), the outer surface of first polysilicon body 124 may be roughened rather than forming a separate hemispherical grain poly layer 110. In this embodiment, the outer surface of first polysilicon layer 124 may be made rough by altering the deposition parameters during formation of first polysilicon body 124. This embodiment results in the same rough surface exhibited by hemispherical grain poly layer 110, without the formation of a separate structural layer.

FIGURES 3A-3D are cross-sectional views of a portion of a partially completed integrated circuit having independently formed array and peripheral isolation dielectrics constructed according to the teachings of the present invention.

Depending on the application and fabrication techniques employed, integrated circuit 10 may, but need not comprise a plurality of trenches and a plurality of moats formed adjacent to the plurality of trenches in semiconductor substrate 12 (not explicitly shown). Trenches and moats may be formed at a variety of points in the fabrication process and by a variety of methods. For example, trenches and moats may be formed contemporaneously with the formation of gate stacks 22 using the same etch used to form gate stacks 22. In that case, the trenches may be filled with a dielectric similar to that used for dielectric isolation region 30 described with reference to FIGURE 1. Alternatively, trenches and moats may be formed by etching away regions of substrate 12 prior to formation of gate stacks 22. In that case, regions of trench dielectric may be disposed within the trenches to substantially fill the trenches. First dielectric layer 20 may then be formed outwardly from substrate 12.

FIGURE 3A shows integrated circuit 10 after formation of a first immediate structure 40 disposed outwardly from first dielectric layer 20. First dielectric layer 20 may be formed outwardly from substrate 12. As described above, trenches and moats may, but need not be formed in substrate 12 prior to formation of first dielectric layer 20. If trenches are formed at that point, regions of trench dielectric may be disposed within the trenches to fill the trenches. Next, floating gate layer 23 may be formed outwardly from first dielectric layer 20. Floating gate layer 23 may comprise, for example, polysilicon or

amorphus silicon. Floating gate layer 23 may later be used to form floating gates 24 of a memory cell array in array region 11 (FIGURE 1).

5 A second dielectric layer 27 may be formed outwardly from floating gate layer 23. Second dielectric layer 27 may comprise any suitable dielectric material or combination of dielectric materials. Second dielectric layer 27 may comprise, for example, oxide, nitride or a heterostructure comprising alternate layers of oxide and nitride. Second
10 dielectric layer 27 may later form second dielectric regions 28 of gate stacks 22 (see FIGURE 1). As described above, second dielectric layer 27 may be scaled to form a dielectric structure having a thickness of approximately 70 Å. Because of such scaling, the capacitance between
15 floating gate 24 and first polysilicon body 26 increases to maintain a constant coupling coefficient. Alternatively, the capacitance between floating gate 24 and first polysilicon body 26 may be increased by forming hemispheric grain poly layer 110 (FIGURE 2) outwardly from floating
20 gate layer 23. Formation of such a layer causes first polysilicon layer 126 to develop a rough surface, thus creating additional surface area, and therefore higher capacitance between floating gate 24 and first polysilicon layer 26.

25 A first polysilicon layer 25 may be formed outwardly from second dielectric layer 27. First polysilicon layer 25 may later form first polysilicon bodies 26 of gate stacks 22. Floating gate layer 23, second dielectric layer 27 and first polysilicon layer 25, collectively form a
30 first intermediate structure 40.

FIGURE 3B shows integrated circuit 10 after the formation of gate stacks 22. Gate stacks 22 may be formed, for example, by masking areas of first intermediate structure 40 where gates stacks are desired. The exposed

areas of first intermediate structure 40 may then be etched away leaving gate stacks 22. Integrated circuit 10 may, but need not comprise trenches in substrate 12 between gate stacks 22 and moats disposed inwardly from gate stacks 22.

5 One method of forming trenches and moats in substrate 12 is to construct them contemporaneously with the fabrication of gate stacks 22. Trenches, moats and gate stacks 22 may be formed, for example, using the same pattern etch used to form gate stacks 22. During this etch, regions of first

10 dielectric layer 20 and substrate 12 residing between gate stacks 22 may be etched away to form trenches between gate stacks 22 and moats inwardly from gate stacks 22.

FIGURE 3C shows integrated circuit 10 during the formation of isolation oxide layer 32 and isolation dielectric layer 34. Isolation oxide layers 32 may be

15 formed, for example, by growing approximately 200 Å of oxide outwardly from gate stacks 22 to provide a good quality oxide layer adjacent to the sidewalls of gate stacks 22. Isolation dielectric layer 34 may be formed,

20 for example, by depositing approximately 0.5 micrometers of oxide outwardly from and between gate stacks 22. If trenches are formed between gate stacks 22 contemporaneously with the formation of gate stacks 22, isolation dielectric layer 34 may also be deposited to fill

25 the trenches. Isolation oxide layer 32 may be formed before or after the deposition of dielectric isolation region 34.

FIGURE 3D shows integrated circuit 10 after portions of isolation oxide layer 32 and isolation dielectric layer

30 34 have been etched away to expose at least an outer surface 29 of first polysilicon layer 26. Remaining portions of isolation oxide layer 32 and isolation dielectric layer 34 between gate stacks 22 comprise dielectric isolation regions 30.

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FIGURES 3A-3D show cross-sectional drawings of a portion of integrated circuit 10 in a direction perpendicular to bit lines (not explicitly shown) which may subsequently be formed using gate stacks 22. Word lines (not explicitly shown) may subsequently be formed perpendicular to the bit lines utilizing gate stacks 22.

FIGURES 4A-4D are schematic diagrams showing cross-sectional views of a series of process steps in the formation of integrated circuit 10, and specifically a gate oxide layer and gate for a peripheral transistor of integrated circuit 10.

FIGURE 4A shows integrated circuit 10 after dielectric isolation regions 30 have been formed between gate stacks 22, and a second polysilicon layer 50 has been disposed outwardly from first polysilicon layer 26 and dielectric isolation layers 30. First polysilicon layer 26 and second polysilicon layer 50 may later form control gates for floating gate memory cells of array region 11.

FIGURE 4B shows integrated circuit 10 after removal of first dielectric layer 20, first intermediate structure 40 and second polysilicon layer 50 from peripheral region 13 of integrated circuit 10. Second polysilicon layer 50 and first intermediate structure 40 may be removed, for example, by masking floating gate array region 11 and etching first intermediate structure 40 and second polysilicon layer 50 from exposed peripheral region 13. First dielectric layer 20 may be removed from peripheral region 13 by, for example, wet deglazing.

FIGURE 4C shows integrated circuit 10 after the formation of a peripheral dielectric layer 60 and a third polysilicon layer 70. Peripheral dielectric layer 60 may be formed outwardly from second polysilicon layer 50 in floating gate array region 11 and outwardly from substrate 12 in peripheral region 13. Peripheral dielectric layer 60

may be formed by any suitable method, such as by deposition or thermal growth. If peripheral dielectric layer 60 is formed through thermal growth, its thickness may be greater in array region 11 than in peripheral region 13. This is due to doping of second polysilicon layer 50, which causes increased growth of thermally grown dielectrics. Peripheral dielectric layer 60 may comprise, for example, oxide or any other suitable dielectric or combination of dielectrics. Third polysilicon layer 70 may be disposed outwardly from peripheral dielectric layer 60. Third polysilicon layer 70 may later form gates of peripheral transistors of integrated circuit 10.

FIGURE 4D shows integrated circuit 10 after the formation of a gate 80 in peripheral region 13. Gate 80 may be formed, for example, by forming a peripheral gate pattern (not shown) outwardly from peripheral dielectric layer 60. The peripheral gate pattern may mask regions of third polysilicon layer 70 outwardly from peripheral region 13, leaving all other areas of third polysilicon layer 70 exposed. Peripheral gates 80 may be formed by etching exposed regions of third polysilicon layer 70 leaving peripheral gates 80 disposed outwardly from peripheral region 13. Sidewall spacers 90 may be formed outwardly from the sidewalls of peripheral gates 80 by any suitable method.

Although the present invention has been described in detail, it should be understood that various changes, substitutions, and alterations can be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method for forming an integrated circuit, comprising:

forming a first dielectric layer disposed outwardly
5 from a semiconductor substrate;

forming a first intermediate structure comprising:

a floating gate layer disposed outwardly from the
first dielectric layer;

a second dielectric layer disposed outwardly from
10 the floating gate layer; and

a first polysilicon layer disposed outwardly from
the second dielectric layer;

removing regions of the first intermediate structure
to form at least one gate stack;

15 forming at least one dielectric isolation region after
the formation of the gate stacks, wherein the at least one
dielectric isolation region is disposed between two gate
stacks.

20 2. The method of Claim 1, wherein forming a
dielectric isolation region comprises:

growing an isolation oxide layer outwardly from the
gate stacks;

25 depositing an isolation dielectric layer outwardly
from and between the gate stacks; and

removing at least a portion of the isolation oxide
layer and the isolation dielectric layer to expose at least
an outer surface of the first polysilicon layer.

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5. The method of Claim 1, further comprising:

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forming trench dielectric regions outwardly from the trenches in the substrate.

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10. The method of Claim 1, further comprising forming a peripheral dielectric layer outwardly from a peripheral region of the substrate, the peripheral region of the substrate disposed adjacent to a region of the substrate supporting the at least one gate stack.

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the dielectric isolation region formed by growing the isolation oxide layer outwardly from the gate stacks; depositing the isolation dielectric layer outwardly from and between the gate stacks; and removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

14. The integrated circuit of Claim 12, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

5 the dielectric isolation region formed by:

growing approximately 200 Å of oxide outwardly from the gate stacks;

depositing approximately 0.5 micrometers of oxide outwardly from and between the gate stacks; and

10 removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

15 15. The integrated circuit of Claim 12, wherein the substrate comprises at least one trench disposed between two gate stacks; and

at least one moat disposed adjacent to the at least one trench and inwardly from the at least one gate stack.

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16. The integrated circuit of Claim 15, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

25 the dielectric isolation region formed by:

growing a layer of oxide outwardly from the gate stacks;

depositing a dielectric outwardly from and between the gate stacks and outwardly from the trenches in the substrate; and

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removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

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18. The integrated circuit of Claim 12, wherein each gate stack further comprises a hemispherical grain poly layer disposed outwardly from the floating gate body.

20. The integrated circuit of Claim 12, further comprising:

a peripheral dielectric layer disposed outwardly from the second polysilicon layer and a peripheral region of the substrate, the peripheral region of the substrate disposed adjacent to a region of the substrate supporting the gate stacks;

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ABSTRACT OF THE DISCLOSURE

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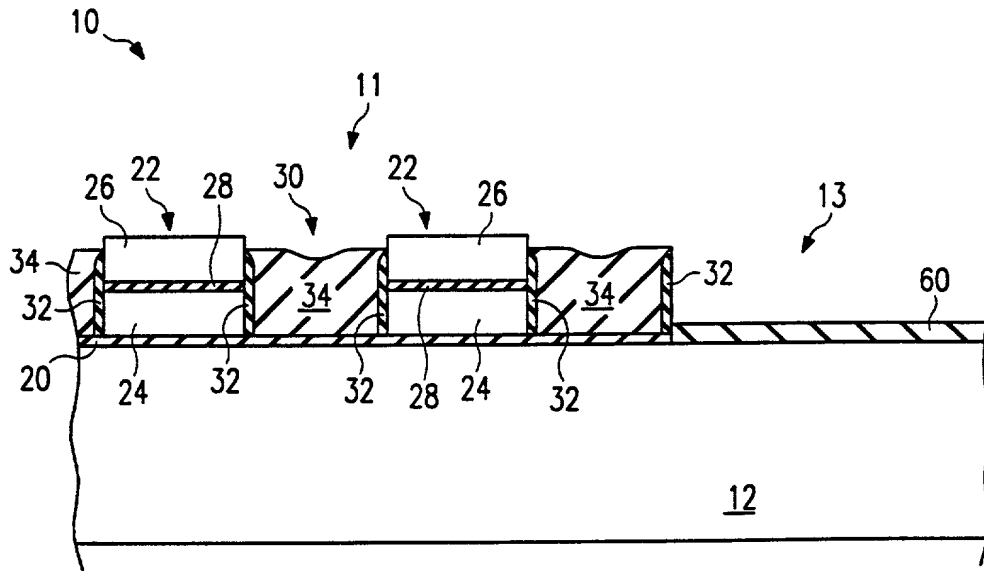


FIG. 1

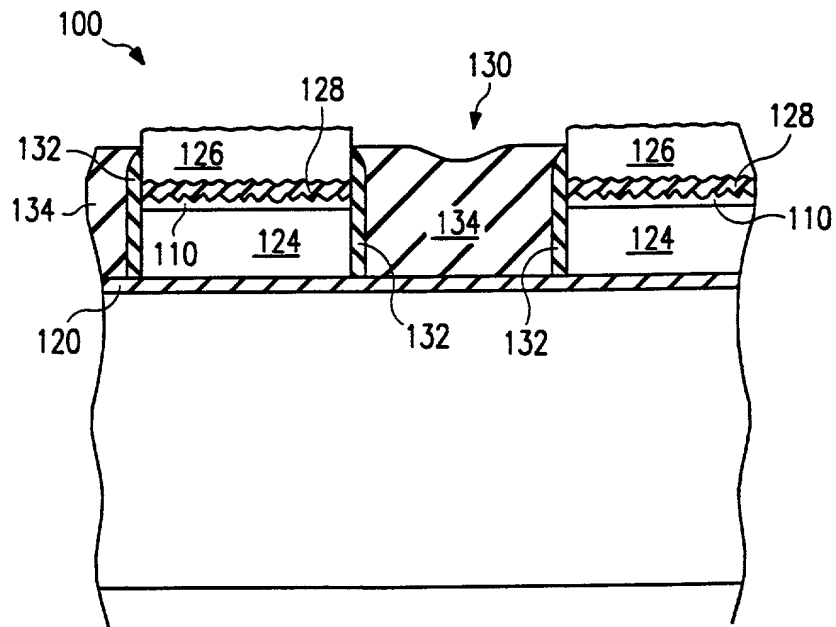


FIG. 2

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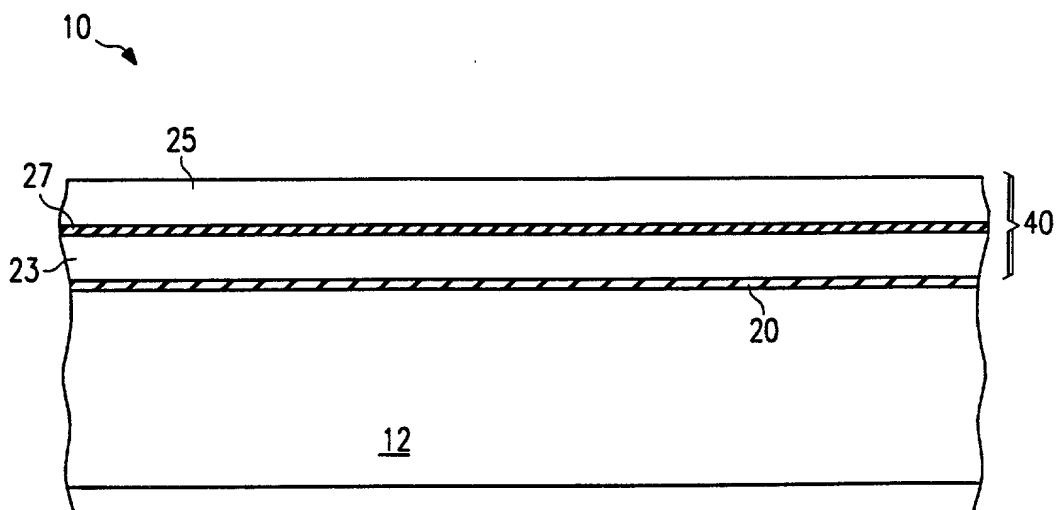


FIG. 3a

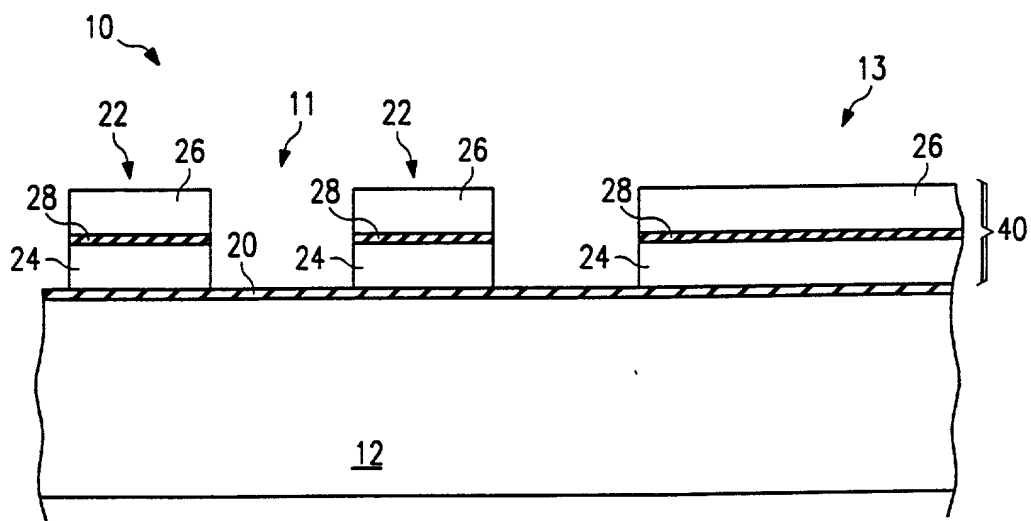


FIG. 3b

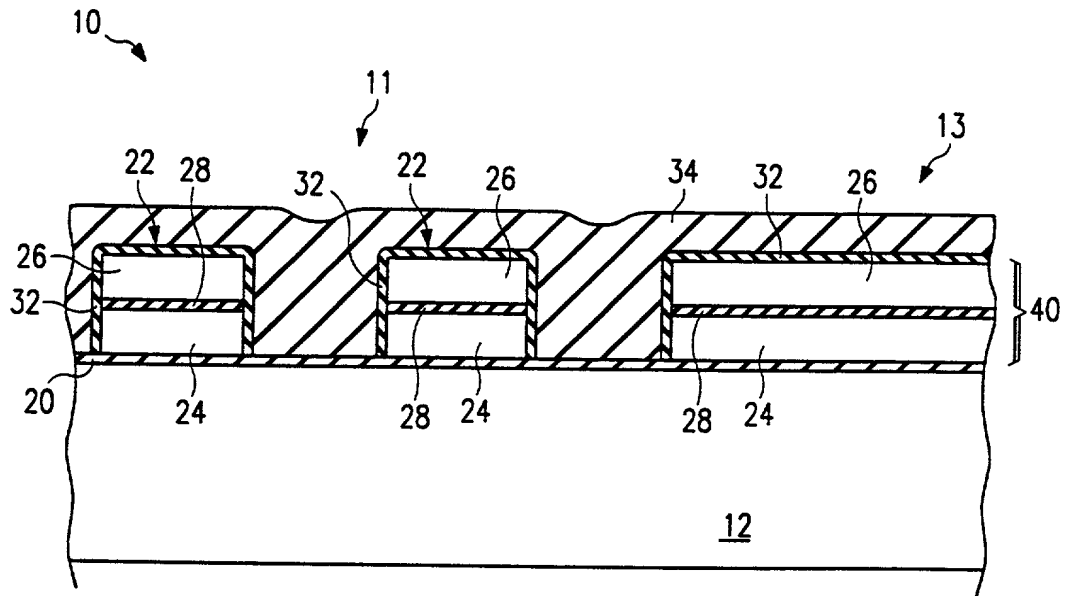


FIG. 3c

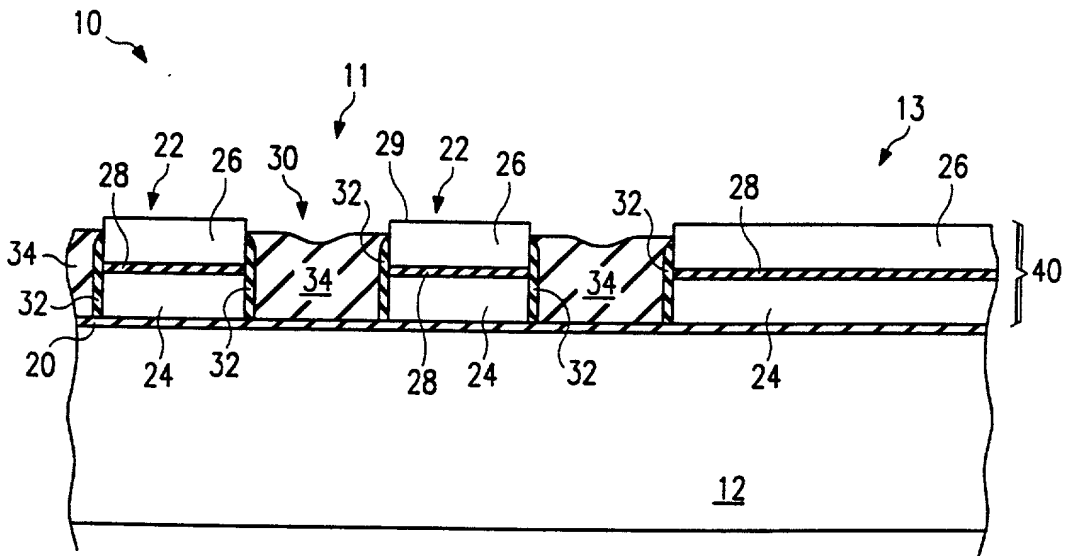


FIG. 3d

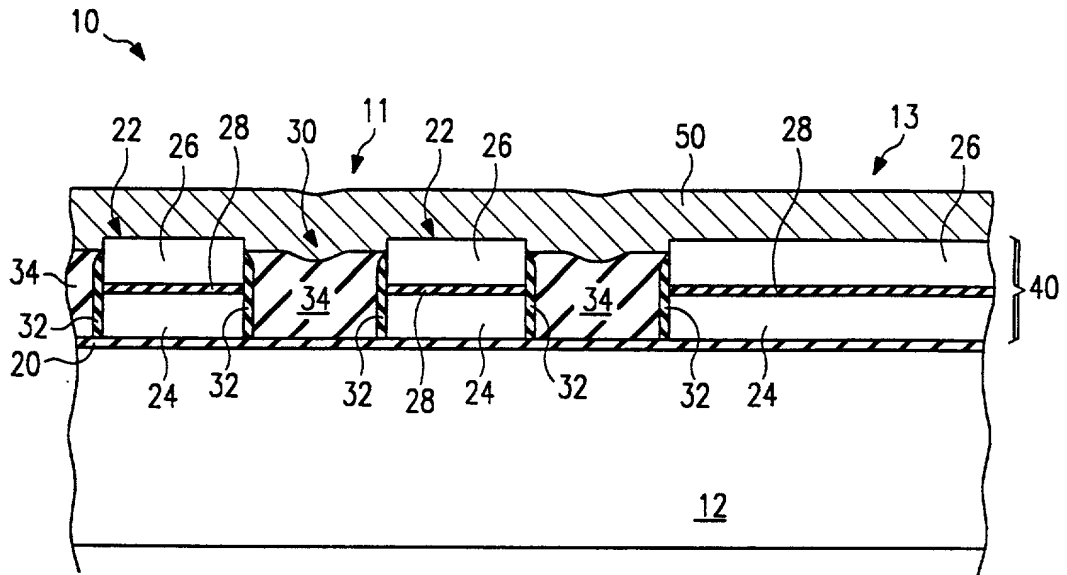


FIG. 4a

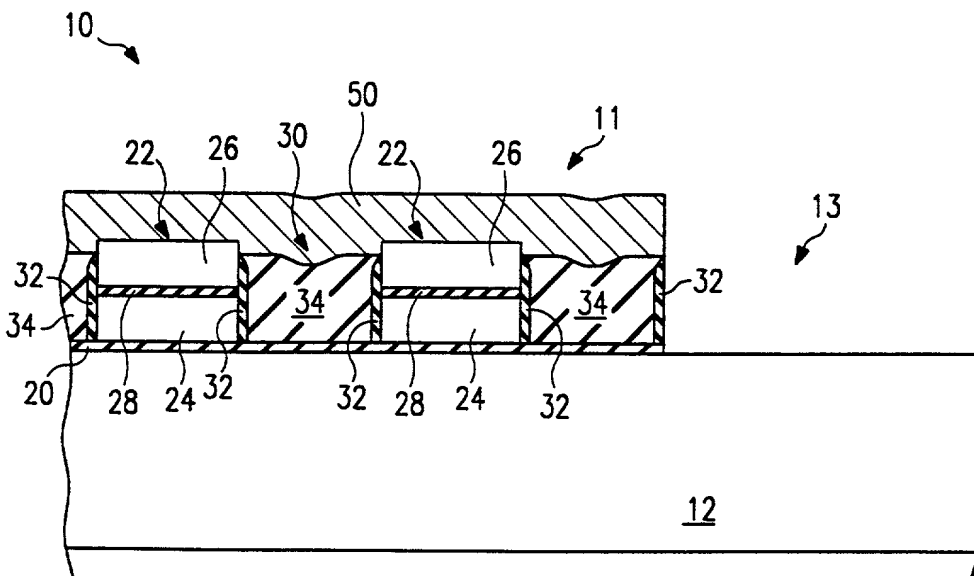
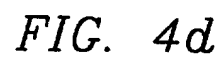
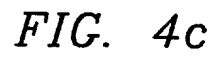


FIG. 4b



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Please send correspondence to:

Jacqueline J. Garner, Esq.
Texas Instruments Incorporated
P. O. Box 655474, M/S 219
Dallas, Texas 75265

and direct telephone calls to:

(973) 278-9697

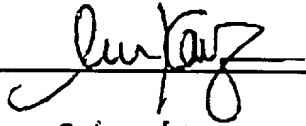
Name of Inventor:
Residence & P.O.

Cetin (nmi) Kaya
9900 Adleta Blvd., #1114
Dallas, Texas 75243

Citizenship:

~~Turkey~~ U.S. CK 9/30/97

Signature of Inventor:

X 
K 9/30/97

Date:

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